Exhibit 5

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD, et al. Defendants.	Civil Case No. 2:22-cv-00293-JRG (Lead Case) **JURY TRIAL DEMANDED**
NETLIST, INC. Plaintiff, v. MICRON TECHNOLOGY, INC., et al. Defendants.	Civil Case No. 2:22-cv-00294-JRG (Member Case) **JURY TRIAL DEMANDED**

DECLARATION OF HAROLD S. STONE, PH.D.,
IN SUPPORT OF MICRON'S CLAIM CONSTRUCTION POSITIONS

TABLE OF CONTENTS

Page

I. INTRODUCTION 3

II. BACKGROUND 4

III. MATERIALS CONSIDERED 6

IV. APPLICABLE LEGAL STANDARDS 6

A. Claim Construction 6

B. Means-Plus-Function Terms 6

V. CLAIM TERMS 8

A. '215 patent 8

B. '417 patent 9

VI. PERSON OF ORDINARY SKILL IN THE ART 11

A. '215 and '417 patents 11

VII. BACKGROUND OF THE TECHNOLOGY 12

A. Computer Memory, Generally 12

B. Non-Volatile Memory, Generally 13

VIII. OVERVIEW OF THE '215 AND '417 PATENTS 14

IX. OPINIONS ON CLAIM CONSTRUCTION 14

A. "logic . . . configured to . . . further configured to . . ." ('215 patent, Claim 1); "logic . . . configurable to . . ." ('417 patent, Claim 1) 15

B. "[. . .]overall CAS latency[. . .]" / "actual operational CAS latency . . ." ('215 patent, Claims 3, 4, 24, 25); "overall CAS latency . . ." / "actual operational CAS latency . . ." ('417 patent, Claim 1) 20

C. "burst of data strobe signals" ('215 patent, Claims 12, 13, 28, 29) 22

D. "circuitry . . . [being] configurable to . . ." / "circuitry includes logic pipelines configurable to . . ." ('417 patent, Claims 1, 6, 11) 23

X. CONCLUSION 27

I, Harold S. Stone, hereby declare as follows:

I. INTRODUCTION

1. My name is Harold S. Stone, Ph.D. I have prepared this declaration as an expert witness on behalf of Micron Technology, Inc., Micron Semiconductor Prods., Inc. and Micron Technology Texas LLC (collectively, "Micron" or "Defendant") in this lawsuit with Plaintiff Netlist, Inc.'s ("Netlist" or "Plaintiff") to provide my analyses and opinions in certain technical aspects of this dispute. In this declaration, I give my analysis and opinions about how a person of ordinary skill in the art at the time of the alleged inventions would have understood certain claim terms in U.S. Patent Nos. 9,858,215 ("the '215 patent") and 11,093,417 ("the '417 patent"). Exs. 1 and 2.

2. This declaration contains statements of my opinions formed to date, and the bases and rationale for these opinions. To the extent Netlist produces one or more expert declarations supporting its positions, I reserve the right to supplement or amend my opinions here upon reviewing such declaration(s). At this time, I have only set forth opinions below as to a subset of the claim terms in dispute. However, I reserve the right to respond to any arguments by Netlist's experts regarding the claim terms, including claim terms for which I have not provided an opinion herein.

3. I provide information helpful to the Court in understanding how a person of ordinary skill in the art ("POSITA") would have understood each claim term at the time of the claimed priority date. For example, for certain terms, my declaration may focus on the understanding of a POSITA in light of textbooks and dictionary definitions, whereas for other terms, my declaration may focus on the understanding of a POSITA in the context of the claims in which the claim terms appear. However, for each claim term, I reserve the right to supplement

or amend my opinions to provide further explanation regarding why additional intrinsic and extrinsic evidence supports a construction, as necessary to respond to Netlist's experts.

4. I am being compensated for the time I have spent on this litigation at my customary rate of $500 per hour. My compensation does not depend in any way upon the opinions I provide or the outcome of this litigation.

II. BACKGROUND

5. Exhibit 3 is a true and correct copy of my *Curriculum Vitae* describing my background and experience. My qualifications generally are set forth in that exhibit. It also includes a list of the publications I have authored and a list of the other cases in which I have testified. I have personal knowledge of the facts and opinions set forth in this declaration, and, if called upon to do so, I would testify competently thereto.

6. I was awarded a Ph.D. and master's degree in Electrical Engineering from the University of California-Berkeley in 1963 and 1961, respectively. I received a Bachelor of Science degree in Electrical Engineering from Princeton University in 1960.

7. After my graduation from Berkeley in 1963, I served as a Research Engineer at Boeing and SRI International. I then held faculty positions at Stanford University and at the University of Massachusetts, where I served as a professor of computer science and electrical engineering.

8. In 1977, together with W. Kahan and J. Coonen, I authored the original proposal ("the KCS proposal") to the working group charged for developing a floating-point standard, which is now known as the IEEE 754 Floating Point Standard. The standard that emerged is that proposal with small changes and additions. It has been implemented in several billion processors.

9. In 1984, I started working for IBM as a Manager of Advanced Architecture Studies. In 1990, I became a Research Staff Member at IBM. During my time at IBM, I managed

and conducted research in the area of memory systems and optical interconnections. I worked at IBM until 1994, when I became a Fellow at the NEC Research Institute, the highest technical position in the company. At NEC, I conducted research in image processing. I am an inventor of a patent to NEC regarding a technique for decompressing JPEG images in a novel way that permits images to be searched without fully decompressing them. The decompression technique is based on inverse discrete cosine transforms, which are one of the basic elements of MPEG decompression.

10. I have authored, coauthored, or edited nine books in various technical areas, the most recent of which appeared in 2011. My textbooks have sold over 100,000 copies. My work on the use of the perfect shuffle interconnections for supercomputers is widely recognized, and many supercomputers based on these interconnections were developed and marketed. For this work and my textbook contributions to the field, I was elected an IEEE Fellow and ACM Fellow, and received the IEEE Piore Field Award, the IEEE Computer Society Taylor Booth Award, and the Charles Babbage Award. I am the principal inventor or co-inventor of 27 patents, including seven in the area of computer architecture: U.S. Patent Nos. 4,989,131; 5,065,310; 5,163,149; 5,611,070; 5,742,785; 5,790,823; and 6,311,260.

11. I have served as a consultant to industry while holding my academic positions and have extensive experience in computer design for embedded computers as a consequence, including low-power computers for use in satellites and ultra-reliable computers for use in nuclear submarine navigation systems. In recent years, I have been a member of two Division Review Committees at Los Alamos National Laboratory in the area of Nuclear Nonproliferation and a consultant to NASA in the area of satellite image processing.

III. MATERIALS CONSIDERED

12. As part of my preparation for writing this declaration, I reviewed the '215 and '417 patents, their prosecution histories (including their provisional applications), the parties' proposed constructions, and respective identification of extrinsic evidence.

IV. APPLICABLE LEGAL STANDARDS

13. I am not an attorney and will not offer opinions on the law, but I have been instructed in and applied the law as described in this section.

A. Claim Construction

14. I have been instructed by counsel on the law regarding claim construction and patent claims and understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to all the limitations recited in the claim from which it depends.

15. It is my understanding that in proceedings before the district court, claim terms are given the ordinary and customary meaning the term would have to a POSITA at the time of the invention, in view of the specification and file history, in the context of the particular claim in which it appears, as well as in light of any other relevant evidence intrinsic and extrinsic to the patent. I am informed that 35 U.S.C. § 112 is applicable law and states, "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention."

B. Means-Plus-Function Terms

16. In addition to claim terms construed according to the principles discussed above, I understand that 35 U.S.C. § 112 of the patent laws allows patent claims to include limitations

expressed as a means for performing a specified function without reciting structure or material for performing that function. I further understand that when this technique is used, such a claim term shall not be construed to cover every conceivable structure for performing the specified function, but rather is construed to cover the structure clearly linked to the function in the patent specification and equivalents thereof. This, I understand, is to avoid claims that are expressed in purely functional terms and are unbounded by any reference to structure in the specification.

17. I understand that a solely functional claim term can include the word "means," and there is a presumption against solely functional claiming in the absence of "means." I further understand a claim limitation lacking the word "means" may also still be a solely functional claim term if the claim fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for performing that function. Thus, if a POSITA understands the words of the claim as lacking a sufficiently definite meaning as a name for structure for performing the specified function, the term is solely functional, and it must be construed to cover the structure clearly linked to the specified function described in the patent specification. For instance, I understand that generic terms such as "module," "mechanism," "element," and "device" are words—referred to as "nonce" words—that can, depending on the circumstances, operate as substitutes for "means" in a solely functional claim term because they typically do not denote sufficiently definite structure for the claimed function. Thus, in construing claim terms, I understand that a threshold question is whether the term is a solely functional term. Using the traditional tools of claim construction I discussed above—including considering the use of the term, if any, in the specification and prosecution history—I understand that one must inquire as to whether a claim term that is potentially a "nonce" word denotes a definite structure in the particular context of the claim. If it does so, then the term is not a solely functional claim term.

18. If, on the other hand, a claim term is determined to be solely functional, I understand that it must be construed through a further two-step process. First, the claimed function must be identified. Next, it must be determined what structure, if any, is clearly linked in the specification to performance of the claimed function. I understand that even if the specification discloses corresponding structure, the disclosure must be of "adequate" corresponding structure to achieve the claimed function. I understand that if a POSITA would be unable to recognize the structure in the specification and a clear link with the corresponding function in the claim, a solely functional claim term is indefinite.

V. CLAIM TERMS

19. I have been informed that the parties dispute the following claim construction positions. I have been asked to consider the meanings that the following claim terms would have had to a POSITA at the time of the inventions of the patents. My opinions on these terms as well as the analysis that informs my opinions is found in Section IX.

A. '215 patent

"logic . . . configured to . . . further configured to . . ." (Claim 1)	
Defendant's Proposed Construction	**Netlist's Proposed Construction**
This is a means-plus-function limitation. **Function** • For claim 1, (i) "respond[ing] to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"; and (ii) further "respond[ing] to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer"	Plain and ordinary meaning.

Corresponding Structure: Indefinite – no corresponding structure.	

"[. . .]overall CAS latency[. . .]" / "actual operational CAS latency . . ." (Claims 3, 4, 24, 25)	
Defendant's Proposed Construction	**Netlist's Proposed Construction**
"the memory module has an overall CAS latency" / "overall CAS latency of the memory module" means "the delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module" "actual operational CAS latency of each of the plurality of memory integrated circuits[/of the memory integrated circuits]" means "the delay between: (1) the time when a read command is executed by each of the plurality of memory integrated circuits[/by the memory integrated circuits], and (2) the time when the first piece of data is made available at an output of each of the plurality of memory integrated circuits [/of the memory integrated circuits]"	Plain and ordinary meaning.

"burst of data strobe signals" (Claims 12, 13, 28, 29)	
Defendant's Proposed Construction	**Netlist's Proposed Construction**
Indefinite.	Plain and ordinary meaning.

B. '417 patent

"circuitry . . . [being] configurable to . . ." / "circuitry includes logic pipelines configurable to . . ." (Claims 1, 6, 11)	
Defendant's Proposed Construction	**Netlist's Proposed Construction**
The identified "circuitry" features in claims 1, 6, and 11 are indefinite. For claim 1, the "circuitry" feature is subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: (i) "transfer[ring] the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal."	Plain and ordinary meaning.

For similar reasons, the "circuitry" features as recited in claims 6 and 11 are indefinite. For example, the "circuitry" feature in claim 6 is subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: (i) the circuitry (of claim 1) "includ[ing] logic pipelines configur[ed] to enable the data transfers between the memory devices and the memory bus through the circuitry." Similarly, the additional "circuitry" feature in claim 11 is subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: (i) "enabl[ing] the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths."	

"logic . . . configurable to . . ." (Claim 1)	
Defendant's Proposed Construction	**Netlist's Proposed Construction**
This is a means-plus-function limitation. **Function** • For claim 1, "output[ting] data buffer control signals in response to the read or write memory command" **Corresponding Structure**: Indefinite – no corresponding structure.	Plain and ordinary meaning.

"overall CAS latency . . ." / "actual operational CAS latency . . ." (Claim 1)	
Defendant's Proposed Construction	**Netlist's Proposed Construction**
"overall CAS latency of the memory module" means "the delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module" "actual operational CAS latency of each of the memory devices" means "the delay between: (1) the time when a read command is executed by each of the memory devices, and (2) the time when the first piece of data is made available at an	Plain and ordinary meaning.

output of each of the memory devices"	

VI. PERSON OF ORDINARY SKILL IN THE ART

20. I understand that a POSITA is a hypothetical person who is presumed to be familiar with the relevant field and its literature at the time of the inventions. I further understand that a POSITA is also a person of ordinary creativity, capable of understanding the scientific principles applicable to the pertinent field. I also understand that in determining the level of ordinary skill in the art of a POSITA, I may consider, among other things, the types of problems encountered in the field, prior solutions to those problems, how quickly innovations are made in the field, the sophistication of the technology, and the levels of education and experience of persons working in the field. I understand that a POSITA is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above.

A. '215 and '417 patents

21. In my opinion, a POSITA at the time of the claimed inventions of the '215 and '417 patents would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Such a person would have been knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and less sophisticated circuits such as tri-state buffers, flip flops, and registers. In the parts of this declaration that relate to the '215 and '417 patents, I use the term "POSITA" to refer to a person

with these or similar qualifications. To have similar qualifications, an individual with additional education or additional industrial experience could still be of ordinary skill in the art if that additional aspect compensates for a deficit in one of the other aspects of the requirements stated above.

22. The basis for my familiarity with the level of ordinary skill is my interaction with large numbers of students seeking related technical degrees over many years of teaching and with people working in the relevant disciplines who were at this level of skill. In reaching this opinion, I have considered the types of problems encountered in the art, the prior art solutions to those problems, the speed with which innovations are made, the maturity of the relevant technology, and the educational and professional levels of people working in the field. In addition, I believe that at the time of the purported invention, I would have qualified as a person of extraordinary skill in the art pertaining to the '215 and '417 patents.

23. My opinions that relate to the '215 and '417 patents are based on the asserted priority date March 5, 2004. In this declaration, I offer no opinion or analysis about whether the March 5, 2004 priority date is correct.

VII. BACKGROUND OF THE TECHNOLOGY

A. Computer Memory, Generally

24. A computer basically consists of an instruction processing unit, which obtains instructions and data from a computer memory and executes those instructions. Such instructions may include operations such as add, multiply, and compare, among many others.

25. The instructions and data are stored in the "main memory." In modern computer systems, main memory consists of dynamic random-access memory ("DRAM"). Information in the memory is identified by its "address," or location. "Random Access" means that any location in the memory can be directly accessed via its address. "Dynamic" refers to the fact that the

memory only remembers its information while power is maintained; if power is turned off, the contents of the DRAMs are lost. Also, for this reason, DRAM is considered volatile memory, i.e., memory that remembers its information only while power is maintained. Further, DRAM chips need to be "refreshed"—the data needs to be periodically read and written back; otherwise, it is lost. DRAM is a semiconductor technology and was invented in the 1960s. DRAM memory consists of semiconductor chips, each of which can hold up to several gigabits of storage, currently up to at least 16 Gb. Over time, the capacity of available DRAM chips increases, as does the speed.

26. DRAM chips are mounted on small printed-circuit boards. The boards that include the DRAM chips are typically referred to as memory modules. A computer may access a memory module to access the DRAM chips on the memory module.

27. DRAM chips and the interfaces to the boards that include the DRAM chips, e.g., memory modules, are standardized so that memories from different vendors can be used in a variety of computers from different manufacturers. The interface standards are developed and promulgated by JEDEC (Joint Electron Device Engineering Council), and include standards such as DDR, DDR2, DDR3, and DDR4.

B. Non-Volatile Memory, Generally

28. Computer memories can be classified as volatile and non-volatile. As described in the previous section, volatile memories, such as DRAM, SRAM, SDRAM, and DDR-DRAM, only store data while powered by the system they are in, and lose the data stored therein when the power is turned off. Non-volatile memories retain their stored data even without power. Examples of non-volatile memories and memory systems include magnetic tape, magnetic and optical drives, read-only memories (ROMs), electrically programmable read-only memories (EPROMs), and electrically erasable programmable read-only memories (EEPROMs).

29. Flash memories are non-volatile EEPROM memories with cells made up of floating gate transistors. Flash memories are erased in blocks and programmed (written to) in portions of a block called a page. For example, a block of flash memory may have 64 pages.

VIII. OVERVIEW OF THE '215 AND '417 PATENTS

30. The '417 patent is a continuation of U.S. Patent No. 10,489,314, which is a continuation of the '215 patent. Accordingly, the '215 and '417 patents share a similar specification. The '215 and '417 patents relate to a "memory module operable to communicate data with a memory controller via a N-bit wide memory bus." '417 patent at Abstract; *see also* '215 patent at Abstract. The memory module may include "a plurality of memory integrated circuits arranged in ranks and including at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, and further comprises a buffer coupled between the at least one first memory integrated circuit and the memory bus and between the at least one second memory integrated circuit and the memory bus." '215 patent at Abstract; '417 patent at Abstract ("The memory module further comprises circuitry coupled between the memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks."). The '215 and '417 patents disclose that by communicating data signals through the data buffer, the '215 and '417 patents purport to "isolate[] one or more of the loads of the memory devices from the computer system." '215 patent at 5:28-29; '417 patent 6:8-9.

IX. OPINIONS ON CLAIM CONSTRUCTION

31. I have been asked to consider the meanings that the following claim terms in subheadings A–D would have had to a POSITA at the time of the inventions of the patents. The following sections present my opinions on these terms as well as the analyses that inform my opinions.

A. "logic . . . configured to . . . further configured to . . ." ('215 patent, Claim 1); "logic . . . configurable to . . ." ('417 patent, Claim 1)

32. I understand that the parties dispute the meaning of the "logic" limitations in the '215 and '417 patents. In claim 1 of the '215 patent, that limitation is as follows:

> logic . . . configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer.

'215 patent at 37:51-61. In claim 1 of the '417 patent, that limitation is as follows:

> logic . . . configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, . . . the logic is further configurable to output data buffer control signals in response to the read or write memory command.

'417 patent, 42:17-40.

33. I understand the parties have proposed the below constructions for these limitations. I will refer to these limitations as the "logic limitation."

Defendant's Proposed Construction	Netlist's Proposed Construction
This is a means-plus-function limitation. **Function** • For claim 1 of the '215 patent, (i) "respond[ing] to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"; and (ii) further "respond[ing] to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer"	Plain and ordinary meaning.

• For claim 1 of the '417 patent, "output[ting] data buffer control signals in response to the read or write memory command" **Corresponding Structure**: Indefinite – no corresponding structure.	

34. I have reviewed the use of the term "logic" in claim 1 of the '215 patent and claim 1 of the '417 patent. The use of "logic" in those claims provides no guidance of specific structure to a POSITA who would understand the term "logic" in those claims to be a generic term that encompasses any hardware, software, or combination that may perform the claimed functions of the logic limitation. In other words, the claim term "logic" does not inform a POSITA of the structural characteristics of the claimed "logic" that is configured to perform the clamed functions of the logic limitation.

35. The remaining claim language of the logic limitation includes functional language that does not inform a POSITA of any structural character of the "logic." For example, the claims do not describe how the "logic" interacts with other claimed components to perform the claimed functionality in a manner that informs a POSITA of the structural character of the term "logic." Specifically, the remaining claim language requires merely that the claimed "logic" be configured to (1) "respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer" and "respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer" in the case of claim 1 of the '215 patent; and (2) "output data buffer control signals in response to the read or write memory command" in the case of claim 1 of the '417 patent. None of this language, nor any other language in the claims of the '215 and

'417 patents, provides any indication of a structure or category of structures narrowing the understanding of a POSITA that any hardware, software, or combination could be used to perform the claimed functions of the logic limitation.

36. I understand that if the Court determines that the logic limitation is a means-plus-function limitation, the limitation will be construed to cover "the corresponding structure, material, or acts described in the specification or equivalents thereof." 35 U.S.C. § 112, ¶ 6.

37. The specifications of the '215 and '417 patents, which share similar specifications, do not describe a corresponding structure for the logic limitation. I have reviewed the portions of the specifications of the '215 and '417 patents that use the term "logic" and variants of that term. The portions of the '215 and '417 patents' specifications that use variants of the term "logic" or similar terms fail to identify a specific structure for performing the claimed functions of the logic limitation. More specifically, the '215 and '417 patents' specifications do not describe any hardware, software, or combination that specifically performs the claimed functions of the logic limitation. As specific examples, the specification does not disclose any structure for the '215 patent claim recital of logic "providing [] control signals to the buffer to enable communication of the [] data burst." Instead, the '215 patent only recites the term "control signals" nine times (excluding recitals in the claims) (emphases added).

- Abstract: "The memory module further comprises logic providing first ***control signals*** to the buffer to enable communication of a first data burst between the memory controller and the at least one first memory integrated circuit through the buffer in response to a first memory command, and providing second ***control signals*** to the buffer to enable communication of a second data burst between the at least one second memory integrated

circuit and the memory bus through the buffer in response to a second memory command";

- 3:47-58: "The logic is configured to respond to the first memory command by providing first ***control signals*** to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer. The logic is further configured to respond to the second memory command by providing second ***control signals*** to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer. The second ***control signals*** are different from the first control signals";
- 6:52-55: "In certain embodiments, the circuit 40 further comprises one or more switches which are operatively coupled to the logic element to receive ***control signals*** from the logic element"; and
- 8:66-9:3: "The one or more switches 120 are operatively coupled to the logic element 122 to receive ***control signals*** from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line."

38. As shown above, none of these recitals provide structural information for the '215 patent logic term function of "providing [] control signals to the buffer to enable communication of the [] data burst." Instead, the recitals merely repeat the functional type language recited in the claim terms at issue or recite switches that receive control signals from the logic.

39. To the extent Examples 1 through 3 of the '215 patent show signals being sent to field effect transistors "FETs," even those disclosures are inadequate because they do not disclose structure to perform the functionality, as recited by the claim.

40. Similarly, the specification does not disclose any structure for the '417 patent claim recital of logic "output[ting] data buffer control signals in response to the read or write memory command" functionality recited in the claims. Instead, the '417 patent only recites the term "data buffer control signals" five times (excluding recitals in the claims) (emphases added):

- Abstract: "The memory module further comprises logic configurable to receive a set of input address and control signals associated with a read or write memory command and output registered address and control signals and ***data buffer control signals***";
- Abstract: "The circuitry is configurable to enable registered transfers of N – bit wide data signals associated with the memory read or write command between the N – bit wide memory bus and the memory devices in response to the ***data buffer control signals*** and in accordance with an overall CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices";
- 3:50-52: "The logic is further configurable to output ***data buffer control signals*** in response to the read or write memory command";
- 4:1-16: "The circuitry is configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the ***data buffer control signals*** and in accordance with an overall CAS latency of the memory module"; and
- 4:23-26: "In some embodiments, the circuitry includes data paths, and the circuitry is configured to enable the data paths in response to the ***data buffer control signals*** so that the N-bit wide data signals are transferred via the data paths."

41. As shown above, none of these recitals provide structural information and instead merely repeat the functional type language recited in the claim terms at issue. Indeed, only two

of these recitals (bullet points one and three above) involve "logic," the rest refer to "circuitry" receiving signals.

42. Specifically, in Examples 1 through 3 of the '417 patent, no data buffer control signals enable communication for buffers with registers. Such structures fall within the scope of Claim 1 of the '417 patent because the claim recites "wherein data transfers through the circuitry are registered."

B. "[. . .]overall CAS latency[. . .]" / "actual operational CAS latency . . ." ('215 patent, Claims 3, 4, 24, 25); "overall CAS latency . . ." / "actual operational CAS latency . . ." ('417 patent, Claim 1)

Defendant's Proposed Construction	Netlist's Proposed Construction
"the memory module has an overall CAS latency" / "overall CAS latency of the memory module" means "the delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module" ('215 patent, Claims 3, 4, 24, 25; '417 patent, Claim 1) "actual operational CAS latency of each of the plurality of memory integrated circuits[/of the memory integrated circuits]" means "the delay between: (1) the time when a read command is executed by each of the plurality of memory integrated circuits[/by the memory integrated circuits], and (2) the time when the first piece of data is made available at an output of each of the plurality of memory integrated circuits [/of the memory integrated circuits]" ('215 patent, Claims 3, 4, 24, 25) "actual operational CAS latency of each of the memory devices" means "the delay between: (1) the time when a read command is executed by each of the memory devices, and (2) the time when the first piece of data is made available at an output of each of the memory devices" ('417 patent, Claim 1)	Plain and ordinary meaning.

43. The '215 and '417 patents' specifications, claims, and prosecution history do not describe the terms "overall CAS latency of the memory module" and "actual operational CAS

latency of each of the memory devices," or their variants recited in the claims. Additionally, these terms are not well-known terms of art.

44. JEDEC standards may help understand what these terms mean. In particular, memory technology in the field of the '215 and '417 patents was (and still is today) developed primarily with an understanding of, and a goal of complying with, the underlying standards associated with that memory technology. Around the 2004–2005 time frame relevant to the '215 and '417 patents, the most relevant standards that a POSITA would have been aware of with respect to the technology of the '215 and '417 patents were standards associated with Double Data Rate (DDR) and DDR2 memory technology.

45. Both DDR and DDR2 standards-related extrinsic evidence supports Micron's constructions. For example, at the time the DDR standard was finalized, CAS latency was generally synonymous with "Read Latency," and the definition for "Read Latency"/CAS Latency (CL) in the DDR standard associated with memory devices is "the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data." *Double Data Rate (DDR) SDRAM Specification*, Standard No. 79, JEDEC Solid State Tech. Corp. (June 2000) (Ex. 4) at 10; *see also id.* at p. 11 (illustrating CAS latency (CL)). Similarly, a DDR standard associated with memory modules, i.e., as opposed to being focused on just the memory devices within the memory module, notes that "[i]n a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency)." *DDR SDRAM Registered DIMM Design Specification*, Standard No. 21-C, JEDEC Solid State Tech. Corp. (Rev. 1.3, Jan. 2002) (Ex. 5) at 68. The remainder of DDR and DDR2 extrinsic evidence is consistent with the foregoing

descriptions. The foregoing clarifies what is meant by the "overall CAS latency"/"actual operational CAS latency" terms and supports Micron's constructions for the terms.

C. "burst of data strobe signals" ('215 patent, Claims 12, 13, 28, 29)

Defendant's Proposed Construction	Netlist's Proposed Construction
Indefinite.	Plain and ordinary meaning.

46. A POSITA would not have understood the meaning of the term "burst of data strobe signals" that is recited in numerous claims of the '215 patent, including at least claims 12, 13, 28, 29, because a POSITA would have considered that the term, as described in the '215 patent's specification, can have multiple meanings, but that the '215 patent's claims do not indicate which meaning of the term is applied in the claims.

47. A POSITA might consider that "burst of data strobe signals" means that each individual strobe signal line includes "a set of consecutively transmitted strobe signals originating from at least two different memory devices." A POSITA might think this because this interpretation would correspond to the "combined strobe" illustrated in FIG. 7 of the '215 patent. This "combined strobe" would be achieved when the strobe pin for a first memory device is tied to the strobe pin for a second memory device, as shown in at least figure 19 of the '215 patent.

48. Alternatively, and equally plausible, a POSITA might consider that "burst of data strobe signals" means that each strobe signal line includes "a set of consecutively transmitted strobe signals originating from a single memory device." A POSITA might think this because this interpretation would correspond to either "strobe a" or "strobe b" illustrated in FIG. 7 of the '215 patent. This "non-combined strobe" would be achieved when the strobe pin for a first memory device is not tied to the strobe pin for a second memory device, as shown in at least figure 1 of the '215 patent.

49. The '215 patent's claims, including the claims that include the term "burst of data strobe signals," do not indicate to a POSITA, with reasonable certainty, which meaning of the term is applied in the claims.

D. "circuitry . . . [being] configurable to . . ." / "circuitry includes logic pipelines configurable to . . ." ('417 patent, Claims 1, 6, 11)

50. I understand that the parties dispute the meaning of the "circuitry" limitations in the '417 patent. In claim 1, that limitation is as follows:

> circuitry . . . being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals.

'417 patent, 42:54-61. In claim 6, that limitation is as follows:

> circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry.

'417 patent, 43:19-22. In claim 11, that limitation is as follows:

> circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths.

'417 patent, 44:10-14.

51. I understand the parties have proposed the below constructions for these limitations. I will refer to these limitations as the "circuitry limitation."

Defendant's Proposed Construction	Netlist's Proposed Construction
The identified "circuitry" features in claims 1, 6, and 11 are indefinite. For claim 1, the "circuitry" feature is subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: (i) "transfer[ring] the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal." For similar reasons, the "circuitry" features as recited in claims 6 and 11 are indefinite. For	Plain and ordinary meaning.

example, the "circuitry" feature in claim 6 is subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: (i) the circuitry (of claim 1) "includ[ing] logic pipelines configur[ed] to enable the data transfers between the memory devices and the memory bus through the circuitry." Similarly, the additional "circuitry" feature in claim 11 is subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of: (i) "enabl[ing] the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths."	

52. I have reviewed the use of the term "circuitry" in claims 1, 6, and 11 of the '417 patent. The use of "circuitry" in those claims provides no guidance of specific structure to a POSITA who would understand the term "circuitry" in those claims to be a generic term that encompasses any hardware, software, or combination that may perform the claimed functions of the circuitry limitation. In other words, the claim term "circuitry" does not inform a POSITA of the structural characteristics of the claimed "circuitry" that is configured to perform the clamed functions of the circuitry limitation.

53. The remaining claim language of the circuitry limitation includes functional language that does not inform a POSITA of any structural character of the "circuitry." For example, the claims do not describe how the "circuitry" interacts with other claimed components to perform the claimed functionality in a manner that informs a POSITA of the structural character of the term "circuitry." Specifically, the remaining claim language specifies merely additional functions that the claimed "circuitry" be configured to perform. None of this language, nor any other language in the claims of the '417 patent, provides any indication of a structure or category of structures narrowing the understanding of a POSITA that any hardware, software, or combination could be used to perform the claimed functions of the circuitry limitation.

54. I understand that if the Court determines that the circuitry limitation is a means-plus-function limitation, the limitation will be construed to cover "the corresponding structure, material, or acts described in the specification or equivalents thereof." 35 U.S.C. § 112, ¶ 6.

55. The specification of the '417 patent does not describe a corresponding structure for the circuitry limitation. I have reviewed the portions of the specification of the '417 patent that use the term "circuitry" and variants of that term. The portions of the '417 patent's specification that use variants of the term "circuitry" or similar terms fail to identify a specific structure for performing the claimed functions of the circuitry limitation. More specifically, the '417 patent's specification does not describe any hardware, software, or combination that specifically performs the claimed functions of the circuitry limitation. As specific examples, the specification does not disclose any structure for transferring data through registered data buffers. So it does not disclose a structure for the "transfer[ring] the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal" functionality recited in claim 1 that also meets the limitation "wherein data transfers through the circuitry are registered. Also it does not disclose any structure for the "logic pipelines configur[ed] to enable the data transfers between the memory devices and the memory bus through the circuitry" functionality recited in claim 6, for lack of disclosure of a circuitry configured for registered data transfers. Nor does it disclose any structure for the "enabl[ing] the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths" recited in claim 11. Instead, the patent only recites the term "data buffer control signals" five times (excluding recitals in the claims) (emphases added):

- Abstract: "The memory module further comprises logic configurable to receive a set of input address and control signals associated with a read or write memory command and output registered address and control signals and ***data buffer control signals***."
- Abstract: "The circuitry is configurable to enable registered transfers of N – bit wide data signals associated with the memory read or write command between the N – bit wide memory bus and the memory devices in response to the ***data buffer control signals*** and in accordance with an overall CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices."
- 3:50-52: "The logic is further configurable to output ***data buffer control signals*** in response to the read or write memory command."
- 4:1-16: "The circuitry is configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the ***data buffer control signals*** and in accordance with an overall CAS latency of the memory module."
- 4:23-26: "In some embodiments, the circuitry includes data paths, and the circuitry is configured to enable the data paths in response to the ***data buffer control signals*** so that the N-bit wide data signals are transferred via the data paths."

56. As shown above, none of these recitals provide structural information and instead merely repeat the functional type language recited in the claim terms at issue. Examples 1 through 3 of the '417 patent do not disclose registered buffers which are required for Claim 1 because of its limitation "wherein the data transfers are registered." Therefore Examples 1 through 3 do not disclose any structure that suffices for the means-plus-function claim elements.

57. Furthermore, it is my opinion that a POSITA would understand that the terms "data paths" and "logic pipelines" simply refer to functional flow of information irrespective of any specific structure for lack of disclosure of structures intended for the registered data transfers recited in Claim 1.

X. CONCLUSION

58. For the reasons stated herein, a POSITA would have agreed with Micron's constructions for the disputed terms and phrases.

I hereby declare that the foregoing is true and correct to the best of my knowledge, subject to the laws of perjury of the United States.

Date: July 13, 2023

Harold S Stone

Dr. Harold S. Stone